REMARKS/ARGUMENTS

Claims 6-25 are pending. Claims 6-10, 13, 14, and 19-21 have been amended. No claim has been added or canceled. No new matter has been added.

Claims 6-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsu in view of Gill and Stewart. Applicant traverses the rejection. Applicant notes that Examiner admits that Hsu and Gill does not disclose, "...first and second memory cells of the plurality of memory cells are programmed by applying a first voltage to the respective control gates of the first and second memory cells, applying a second voltage to the respective sources of the first and second memory cells and grounding the respective drains of the first and second memory cells..."

The Examiner uses Stewart to remedy the above deficiencies of Hsu and Gill. However, Stewart discloses a non-volatile device that is configured differently and is not compatible with the devices of Hsu and Gill. In Hsu and Gill, each memory cell has only one transistor (see Fig. 2 of Hsu and Fig. 1B of Gill). Stewart uses at least two transistors (Fig. 4). Stewart states, "Fig. 4 is an equivalent schematic diagram of one cell of the array of Fig. 1 (col 1:61-62)."

To program the memory cell of Stewart two transistors Pw and Ps need to be turned on. Pw transistor is turned on to apply a voltage to the source region. Note this source region accordingly is not coupled to "a common node," as recited in claim 6.

On the other hand, each memory cell of Hsu and Gill only has a single transistor so two transistors cannot be turned on during the programming operation. The Examiner attempts to borrow certain programming features from Stewart to remedy the deficiencies of Hsu and Gill while ignoring the above programming feature and configuration of Stewart. Such a "pick-and-choose" approach is improper use of hindsight based on the teaching of the present inventor.

In addition, the Examiner asserted that the Pw transistor of Stewart is "a normal nonvolatile memory device and Hsu and Gill do disclose this transistor..." This is incorrect. Hsu and Gill do not disclose such a transistor. Hsu and Gill disclose single-transistor memory

cells whereas Stewart discloses two-transistor memory cells, the Pw transistor being one of those two transistors. Therefore, Hsu and Gill cannot disclose such a transistor as the Examiner asserts. Claim 6 is allowable for at least for the reasons set forth above. Claims 7-13 depend from claim 6 and is allowable at least for this reason.

Claim 14 recites, "...the control gate is applied with a first voltage and the source region is applied with a second voltage to program the non-volatile device, wherein the floating gate, control gate, drain region, and source region together define a first memory cell that is configured to store one bit of data, wherein the non-volatile device further includes a second memory cell that is configured to store one bit of data, the second transistor including a source region that shares a common node with the source region of the first memory cell." The cited references do not disclose or suggest the above recited features. Claim 14 is allowable at least for this reason. Claims 15-18 depend from claim 14 and are allowable at least for this reason.

Claim 19 recites, "...the memory cell including: a floating gate overlying a surface of the substrate, a control gate overlying the floating gate and being electrically coupled to a first conductive line extending in a first direction, a first conductive region provided in the substrate and proximate a first end of the floating gate, the first conductive region extending a first distance into the substrate and having a first graded profile relative to the surface of the substrate, the first conductive region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and a second conductive region provided in the substrate and proximate a second end of the floating gate, the second conductive region being a double-diffused region that extends a second distance into the substrate and having a second graded profile relative to the surface of the substrate, the second distance being greater than the first distance, the second graded profile having a greater slope relative to the surface of the substrate than the first graded profile, wherein the control gate is applied with a first voltage and the second conductive region is applied with a second voltage to program the non-volatile device, the second voltage being a positive voltage, wherein the memory cell is defined by a single transistor." The cited references do not disclose or suggest the above recited features. Claim 19 is allowable at least for this reason. Claims 20-25 depend from claim 19 and are allowable at least for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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